REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

Claim 1 has been amended to incorporate the subject matter of claim 4, and claim 4 has been canceled. Additional support for the amendment of claim 1 is provided at least in paragraphs [0015] and [0041] of the specification.

Claims 1-5 and 8 were rejected, under 35 USC §103(a), as being unpatentable over Yamauchi (US 6,128,253) in view of Okamura (US 5,521,541). Claims 6 and 9 were rejected, under 35 USC §103(a), as being unpatentable over Yamauchi in view of Okamura and McElvain et al. (US 2006/0095872). Claim 7 was rejected, under 35 USC §103(a), as being unpatentable over Yamauchi in view of Okamura and Meier et al. (US 6,854,567). To the extent these rejections may be deemed applicable to the amended claims, the Applicants respectfully traverse based on the points set forth below.

Amended claim 1 recites (1) a scan clock circuit, for providing a scan clock to a plurality of flip-flop circuits which configure a scan chain, (2) a separate clock circuit for providing normal clocking operation of the flip-flop circuits, and (3) a lattice-shaped wiring portion for the scan clock

circuit and a tree-shaped transmission path configuration for the normal operation clock circuit.

An advantage of a lattice-shaped wiring portion for the scan clock circuit is to prevent the generation of a differential delay (i.e., clock skew) resulting from factors that may not be detected by simulation in a micro fabrication process, such as manufacturing variation and delay calculation error. However, the power consumption for a lattice-shaped wiring portion is higher than that for a tree-structure wiring portion, and the timing restriction of the clock circuit for normal operation, when data is shifted, is not as strict as that for the scan clock circuit. Therefore, to reduce power consumption, the clock circuit for normal operation is configured as a tree structure.

Claim 1 recites two separate clock circuits, one configured with lattice-shape wiring for providing clock to a plurality of flip-flop circuits of a scan chain and another configured with tree-shaped transmission paths for normal clocking operation of the flip-flop circuits. With two separate clock circuits, an advantage is provided in that the claimed invention may prevent the above-mentioned clock skew and a resulting malfunction of the circuit during a scan test.

Although Yamauchi discloses a "normal clock input terminal 101" and a "test clock input terminal 102," as suggested in the

Office Action (see Office Action page 2, second to last paragraph), Yamauchi provides no description of a clock circuit for normal operation or a clock circuit for scanning operation, as recited in claim 1.

Further, while Okamura may disclose lattice-shaped wiring for a clock signal, as suggested in the Office Action, (see Office Action page 3, lines 7-8), Okamura does not suggest clock signal wiring for normal operation that is separate from the clock signal wiring used for scanning operation, as recited in claim 1.

Moreover, Okamura does not disclose the claimed combination of one clock circuit configured with lattice-shape wiring for providing clock to a plurality of flip-flop circuits of a scan chain and another separate tree-shaped transmission path configuration for normal clocking operation of the flip-flop circuits.

As a result, even if Yamauchi's device were modified in light of Okamura's teachings, the result still would not achieve the Applicants' claimed structure or the above-described advantages derived therefrom.

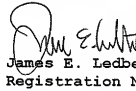
Accordingly, the Applicants respectfully submit that Yamauchi and Okamura, considered individually or in combination, do not render obvious the subject matter defined by claim 1.

Therefore, allowance of claim 1 and all claims dependent therefrom is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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